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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,312	12/06/2001	Katsuaki Isobe	001701.00129	7010

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/003,312	Applicant(s) ISOBE ET AL.	
	Examiner An T. Luu	Art Unit 2816	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-15* is/are allowed.

6)☒ Claim(s) *1-10 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/505,204* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's Amendment filed on 7-21-03 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 6-7 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by the You reference (U.S. Patent 5,319,253).

Park discloses in figure 6 an apparatus comprising a clock inverter circuit 100B receiving a first pulse signal (WL) for outputting a second pulse signal (output of INV38) having a pulse width greater than a pulse width of the first pulse signal (by means of INV34-38); and a logic circuit (NOR 39) receiving the second pulse signal an inverted signal of the first pulse signal (output of 33) wherein the NOR 39 outputs a third pulse signal having a shorter pulse width than that of the second pulse signal as required by claims 1-2. It is noted that the third pulse signal will have a longer pulse width than that of the second pulse signal if the second pulse signal has a pulse width shorter than a pulse width of the first pulse signal because the third pulse is a NORing function of the first pulse signal and its delayed version. Consequently, the trailing edge of the third pulse is determined by delayed version of the first pulse signal (output of the clock inverter circuit).

As to claims 6-7 and 16-17, the scopes of them are similar same as those of claims 1 and 2. Therefore, they are rejected for the same reason set forth above.

As to claims 18-19, figure 6 discloses a first delay element 100 and a second delay element 200 in series to the first delay element wherein each delay element has the same structure as required by claim 1.

3. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by the Cha reference (U.S. Patent 5,723,993).

Cha discloses in figure 2 an apparatus comprising a clock inverter circuit (inverters 11-18) receiving a first pulse signal (IN) for outputting a second pulse signal (N2) having a pulse width greater than a pulse width of the first pulse signal (by means of INV12-18) in response to the first pulse only; and a logic circuit (NAND 19) receiving the second pulse signal an inverted signal of the first pulse signal (output of 11) wherein the NAND 19 outputs a third pulse signal (OUT) having a shorter pulse width than that of the second pulse signal as required by claim 20.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the You reference (U.S. Patent 5,319,253).

You discloses all the claim invention except for explicitly showing a NAND gate in his logic circuit. However, it is known in the art that NAND and NOR logic gates are used to change a duty cycle of a signal (i.e., changing pulse width) in which NAND gate is commonly used for

lengthen the pulse wherein NOR gate is commonly used for shorten the pulse. Therefore, it would have been obvious to one skilled in the art to replace a NOR gate with a NAND gate, or vice versa, in You inventive circuit so that the pulse width would be changed to a desired width to meet the requirement of application. Further, the leading edge of the third pulse is determined by delayed version of the first pulse signal (output of the clock inverter circuit) by NANDing function.

6. Claims 4-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the You reference (U.S. Patent 5,319,253) in view of the D'Souza et al. reference (U.S Patent 5,605,270).

You discloses all the claimed invention including a delay circuit comprising series connected inverters. You does not disclose an inverter having a specifically configuration as recited in claim 4 and 5 of the instant application. D'Souza et al discloses in figure 3 an inverting apparatus comprising NMOS and PMOS transistors having different channel widths (i.e. 20 vs. 0.6) and a ratio of the driving capability of the PMOS transistor to that of the NMOS transistor is different from one to another, and the rise time of a pulse signal is different from a decay time of the pulse signal (i.e., 20/0.6 for PMOS and 10/0.6 for NMOS). It would have been obvious to one skilled in the art to replace a generic delay circuit in You with series-connected inverters each having a series-connected PMOS and NMOS transistors as taught by D'Souza. A skilled artisan would have been motivated to combine these arts to reduce current leakage and to improve noise immunity or to change duty cycle (i.e., by varying the rising time and falling time of a signal.)

As to claims 8-10, the scopes of these claims are similar to those of claims 2-5, respectively. Therefore, they are rejected for the similar reasons set for above.

Response to Arguments

7. Applicant's arguments filed 7-21-2003 have been fully considered but they are not persuasive.

Regarding the rejection of claims 1, 16 and 17 under 35 USC 102, Applicant has argued that You's circuit depends on the detection signal (ΦDR), and not the input signal (ΦWL) wherein Applicant's invention calls for a circuit depending on the input signal. Examiner respectfully disagrees with the above assertion since You's circuit depends upon both of the signals. It is noted that the recitation of claim 1 does not call for the fact that *the input signal is the only signal being provided for the apparatus.*

Regarding to the rejection of claims 4-5 and 8-10 under 35 USC 103, Applicant has argued that D'Souza fails to remedy the deficiencies of You. Examiner respectfully disagrees since D'Souza is not for remedy the deficiencies of You. Rather, it is used in combination of You to provide different aspect to improve what has been taught in You. You teaches a delay, including generic inverters, having output signal characterized that its pulse width is different from its input signal by means of NAND gate (i.e., logic 35 or 55 to vary pulse width by means of detection signal (ΦDR) wherein the delay of each inverter is seen to be indifferent). D'Souza teaches an inverter being configured in a specific way to reduce current leakage and to improve noise immunity or to change duty cycle (i.e., by varying the rising time and falling time of a signal). Therefore, the combination of You and D'Souza is proper.

Allowable Subject Matter

8. Claims 11-15 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claim 11. Specifically, none of the prior art teaches or fairly suggests, among other things, limitations "a first delay line", "a second delay line" and "a state holding section" as recited on lines 2-8.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 703-308-4922. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

An T. Luu ATL
8-12-2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800